Claims

What is claimed is:

1. A metal-oxide-semiconductor (MOS) device, comprising:

a semiconductor layer of a first conductivity type;

a source region of a second conductivity type formed in the semiconductor layer;

a drain region of the second conductivity type formed in the semiconductor layer and spaced apart from the source region;

a gate formed proximate an upper surface of the semiconductor layer and at least partially between the source and drain regions;

a buried lightly-doped drain (LDD) region of the second conductivity type formed in the semiconductor layer between the gate and the drain region, the buried LDD region being spaced laterally from the drain region; and

a second LDD region of the first conductivity type formed in the buried LDD region and proximate the upper surface of the semiconductor layer, the second LDD region being self-aligned with the gate and spaced laterally from the gate such that the gate is non-overlapping relative to the second LDD region.

2. The device of claim 1, further comprising a shielding structure formed proximate the upper surface of the semiconductor layer and at least partially between the gate and the drain region, the shielding structure being electrically connected to the source region, the shielding structure being spaced laterally from the gate and being substantially non-overlapping relative to the gate.

3. The device of claim 2, wherein the shielding structure is formed substantially concurrently with the gate.

4. The device of claim 2, wherein a first insulating layer under the gate and a second insulating layer under the shielding structure are formed of different thicknesses in comparison to one another.

5. The device of claim 1, wherein the device comprises a diffused MOS (DMOS) device.

6. The device of claim 5, wherein the device comprises a lateral DMOS (LDMOS) device.

7. The device of claim 5, wherein the device comprises a vertical DMOS device.

8. The device of claim 1, wherein the buried LDD region is formed in the semiconductor layer at a depth in a range from about 0.5 micron to about two microns, and the second LDD region is formed in the semiconductor layer at a depth in a range from about 0.05 micron to about 0.5 micron.

9. The device of claim 1, further comprising an alignment structure formed proximate the upper surface of the semiconductor layer and at least partially between the second LDD region and the drain region, wherein the drain region is self-aligned to a first edge of the alignment structure and the second LDD region is self-aligned with a second edge of the alignment structure such that the second LDD region is self-aligned with the drain region.

10. An integrated circuit including at least one metal-oxide-semiconductor (MOS) device, the at least one MOS device comprising:

a semiconductor layer of a first conductivity type;

a source region of a second conductivity type formed in the semiconductor layer;

a drain region of the second conductivity type formed in the semiconductor layer and spaced apart from the source region;

a gate formed proximate an upper surface of the semiconductor layer and at least partially between the source and drain regions;

a buried lightly-doped drain (LDD) region of the second conductivity type formed in the semiconductor layer between the gate and the drain region, the buried LDD region being spaced laterally from the drain region; and

a second LDD region of the first conductivity type formed in the buried LDD region and proximate the upper surface of the semiconductor layer, the second LDD region being self-aligned with the gate and spaced laterally from the gate such that the gate is non-overlapping relative to the second LDD region.

11. The integrated circuit of claim 10, wherein the at least one MOS device further comprises a shielding structure formed proximate the upper surface of the semiconductor layer and at least partially between the gate and the drain region, the shielding structure being electrically connected to the source region, the shielding structure being spaced laterally from the gate and being substantially non-overlapping relative to the gate.

12. The integrated circuit of claim 10, wherein the at least one MOS device further comprises an alignment structure formed proximate the upper surface of the semiconductor layer and at least partially between the second LDD region and the drain region, wherein the drain region is self-aligned to a first edge of the alignment structure and the second LDD region is self-aligned with a second edge of the alignment structure such that the second LDD region is self-aligned with the drain region.

13. A method of forming a metal-oxide-semiconductor (MOS) device, the method comprising the steps of:

forming a buried lightly-doped drain (LDD) region of a first conductivity type in a semiconductor layer of a second conductivity type;

forming a gate on an upper surface of the semiconductor layer;

forming a second LDD region of the second conductivity type in the buried LDD region and proximate the upper surface of the semiconductor layer, the second LDD region being

self-aligned with the gate and spaced laterally from the gate such that the gate is non-overlapping relative to the second LDD region; and

forming source and drain regions of the first conductivity type in the semiconductor layer, the gate being formed at least partially between the source and drain regions.

14. The method of claim 13, wherein the step of forming the second LDD region comprises the steps of:

forming a shielding structure on a least a portion of the insulating layer at least partially between the gate and the drain region, the shielding structure being self-aligned to the gate; and

forming the second LDD region in the buried LDD region such that the second LDD region is self-aligned to the shielding structure.

15. The method of claim 14, further comprising the step of removing the shielding structure after forming the second LDD region.

16. The method of claim 15, wherein the step of removing the shielding structure comprises etching at least the shielding structure.

17. The method of claim 14, further comprising the steps of:

removing the shielding structure;

removing at least a portion of an insulating layer under the shielding structure; and

forming a new shielding structure on at least a portion of the insulating layer on which the removed shielding structure was formed.

18. The method of claim 14, wherein the shielding structure is formed substantially concurrently with the gate.

19. The method of claim 14, further comprising the step of forming an electrical connection between the shielding structure and the source region.

20. The method of claim 13, further comprising the step of forming an alignment structure on the insulating layer and at least partially between the gate and the drain region, the drain region and the second LDD region being self-aligned with the alignment structure.

21. The method of claim 20, further comprising the step of removing the alignment structure after forming the second LDD region and drain region.

22. The method of claim 20, wherein the alignment structure is formed substantially concurrently with the gate.

23. The method of claim 13, wherein the buried LDD region is formed in the semiconductor layer at a depth in a range from about 0.5 micron to about two microns, and the second LDD region is formed in the semiconductor layer at a depth in a range from about 0.05 micron to about 0.5 micron.

24. The method of claim 13, wherein the MOS device is a diffused MOS (DMOS) device.